A2 -- Figure 4 is a flow diagram showing process steps that may be implemented in a computer system, according to an embodiment of the invention. --

Please add the following new paragraph after the paragraph beginning at page 9, line 14:

A3 -- Figure 4 shows a process 400 used by a computer system, according to an embodiment of the invention. In step 410, a data access is made by the CPU or a peripheral device. In step 420, the data access is routed to the main memory. In step 430, a control/status access is made by the CPU or a peripheral device. In step 440, the control/status access is routed to the multi-ported memory. According to some embodiments, the process steps of Figure 4 may be implemented by the instructions of an article comprising a computer-readable medium which stores computer-executable instructions for memory accessing. --

In the claims:

Please cancel claim 9.

Please amends claims 1, 6, 10, 14, 18, 19, 21, 23, 27, and 29 as follows:

-- 1. (Amended) A computer system, comprising:

a non-cached multi-ported memory;

a main memory;

a central processing unit coupled to the multi-ported memory;

a bus configured to communicate with one or more peripheral devices, the bus coupled to the multi-ported memory and configured to access the multi-ported memory independently of the central processing unit;

wherein the computer system is configured so that control accesses from the central processing unit are directed to the multi-ported memory and data accesses from the central processing unit are directed to the main memory.

6. (Amended) The system of claim 1, wherein the multi-ported memory is chosen from the group consisting of static random access memory and dynamic random access memory.

10. (Amended) A method comprising:

routing a data access from a peripheral device to a first memory in the computer; and

routing a status access from a peripheral device to a second memory in the computer.

A7

14. (Amended) An article comprising a computer-readable medium which stores computer-executable instructions for memory accessing, the instructions causing a machine to:

route a data access from a peripheral device to a first memory in the computer; and

route a status access from the peripheral device to a second memory in the computer.

18. (Amended) The article of claim 14, wherein the second memory is dual-ported.

A8

19. (Amended) A method comprising:

routing ~~the~~ a data access from a central processing unit to a first memory in the computer; and

routing a control access from the central processing unit to a second memory in the computer.

A9

21. (Amended) The method of claim 19, wherein the second memory is included in a memory controller.

A10

23. (Amended) An article comprising a computer-readable medium which stores computer-executable instructions for memory accessing, the instructions causing a machine to:

route a data access from a central processing unit to a first memory in the computer; and

route a control access from the central processing unit to a second memory in the computer.

27. (Amended) An integrated circuit comprising:

a memory controller configured to communicate with a CPU, a peripheral device, and a main memory, the memory controller including a multi-ported memory, wherein control accesses for the CPU are directed to the multi-ported memory and wherein data accesses for the CPU are directed to the main memory.

29. (Amended) The integrated circuit of claim 27, wherein the multi-ported memory is chosen from the group consisting of static random access memory and dynamic random access memory. --

Please add claims 31-33.

-- 31. (New) The system of claim 1, wherein the computer system is further configured so that status accesses from a peripheral device are directed to the multi-ported memory and data accesses from the peripheral device are directed to the main memory

32. (New) The integrated circuit of claim 27, wherein data accesses from the peripheral device are directed to the main memory.

33. (New) The integrated circuit of claim 27, wherein status accesses from the peripheral device are directed to the multi-ported memory. --